Lpddr4 sdram datasheet



 #define CONFIG_SYS_SDRAM_BASE
 0x4000000

 #define PHYS_SDRAM
 0x40000000

 #resize DRAM here
 0xC0000000 /* 3GB DDR *

 //#define PHYS_SDRAM_SIZE
 0xC0000000 /* 3GB DDR *

 #define PHYS_SDRAM_SIZE
 0x100000000 /* 4GB DDR *

 #define CONFIG_NR_DRAM_BANKS
 1

NXP Semiconductors Data Sheet: Technical Data Document Number: IMX9MDOLOIEC Rev. 1.1,07/2019

 MMX28M07CVAHZAA
 MMX28M07CVAHZAA

 MMX28M02CVAHZAA
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i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processors Data Sheet for Industrial Products



Cardering in tormation See Table 2 on gage 6

1 i.MX 8M Dual / 8M QuadLite / 8M Quad introduction

I he iM XSM Dual/SM Quad Line /SM Quad pro cases a represent NXP's latest market of connected streaming audio/hideo devices, scanningfinaging devices, and 2. Modules 13 various devices requiring high-performance, low-power pro cases 5.

The iM XSM Dual/SM QuadLin /SM Quad processors feature advanced implementation of a quad Am00 CortanD-A33 come, which operates at speeds of up to 1.3 GHr. A general purpose CortanD-M4 come processor is for low-power processing. The DRAM controllar support 32-bit/16-bitLPDDB4, DDB4, and DDB3L memory. Them are a number of other interfaces for connecting paripherals, such as WLAN, Bluetooth, GPS, displays, and camera sensors. The iM X SM Quad and i MX SM Dual processors have hardware acceleration for video physicals up to 4K, and candring the video outputs up to 60 fps. Although the i MX SM QuadLins processor does not have hardware acceleration for video decode, it allows for video physical with so flware decoders if meeded.



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Lpddr4 sdram vs ddr4. Lpddr4 vs sdram.

Serial NOR Flash (QSPI, SPI) Den Part Number Buy Type Vcc Frequency Temp.Range Package Type Status Models Alt. Version/Doc 512K IS25LQ512B Multi I/O Quad SPI 2.3-3.6V 33M/104Mhz -40 to 125°C SOIC, TSSOP, WSON, VVSOP, USON Prod IBIS/Verilog IS25CD512 1M IS25LP010E Multi I/O Quad SPI 2.3-3.6V 50M/104Mhz -40 to 125°C SOIC, TSSOP, WSON, VVSOP, USON Prod IBIS/Verilog IS25CD512 1M IS25LP010E Multi I/O Quad SPI 2.3-3.6V 50M/104Mhz -40 to 125°C SOIC, TSSOP, WSON, VVSOP, USON Prod IBIS/Verilog IS25CD512 1M IS25LP010E Multi I/O Quad SPI 2.3-3.6V 50M/104Mhz -40 to 125°C SOIC, TSSOP, WSON, VVSOP, USON Prod IBIS/Verilog IS25CD512 1M IS25LP010E Multi I/O Quad SPI 2.3-3.6V 50M/104Mhz -40 to 125°C SOIC, TSSOP, WSON, VVSOP, USON Prod IBIS/Verilog IS25CD512 1M IS25LP010E Multi I/O Quad SPI 2.3-3.6V 50M/104Mhz -40 to 125°C SOIC, TSSOP, WSON, VVSOP, USON Prod IBIS/Verilog IS25CD512 1M IS25LP010E Multi I/O Quad SPI 2.3-3.6V 50M/104Mhz -40 to 125°C SOIC, TSSOP, WSON, VVSOP, USON Prod IBIS/Verilog IS25CD512 1M IS25LP010E Multi I/O Quad SPI 2.3-3.6V 50M/104Mhz -40 to 125°C SOIC, TSSOP, WSON, VVSOP, USON Prod IBIS/Verilog IS25CD512 1M IS25LP010E Multi I/O Quad SPI 2.3-3.6V 50M/104Mhz -40 to 125°C SOIC, TSSOP, WSON, VVSOP, USON Prod IBIS/Verilog IS25CD512 1M IS25LP010E Multi I/O Quad SPI 2.3-3.6V 50M/104Mhz -40 to 125°C SOIC, TSSOP, WSON, VVSOP, USON Prod IBIS/Verilog IS25CD512 1M IS25LP010E Multi I/O Quad SPI 2.3-3.6V 50M/104Mhz -40 to 125°C SOIC, TSSOP, WSON Prod IBIS/VERILOG IS25CD512 1M IS25LP010E MULTI I/O QUAD SPI 2.3-3.6V 50M/104Mhz -40 to 125°C SOIC, TSSOP, WSON Prod IBIS/VERILOG IS25CD512 1M IS25LP010E MULTI I/O QUAD SPI 2.3-3.6V 50M/104Mhz -40 to 125°C SOIC, TSSOP, WSON PROD IS25CD512 1M IS25LP010E MULTI I/O QUAD SPI 2.3-3.6V 50M/104Mhz -40 to 125°C SOIC, TSSOP, WSON PROD IS25CD512 1M IS25LP010E SOIC,TSSOP,WSON,VVSOP,USON Prod IBIS/Verilog IS25LQ010B 2M IS25LP020E Multi I/O Quad SPI 2.3-3.6V 50M/104Mhz -40 to 125°C SOIC,TSSOP,WSON,VVSOP,USON Prod IBIS/Verilog IS25LQ020B IS25WP020E Multi I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25LQ020B IS25WP020E Multi I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25LQ020B IS25WP020E Multi I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25WP020E Multi I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25WP020E Multi I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25WP020E Multi I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25WP020E Multi I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25WP020E Multi I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25WP020E Multi I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25WP020E Multi I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25WP020E Multi I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25WP020E Multi I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25WP020E Multi I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25WP020E Multi I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25WP020E Multi I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25WP020E Multi I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25WP020E MULti I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25WP020E MULti I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/Verilog IS25WP020E MULti I/O Quad SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod IBIS/VERILOG IS25WP020E MULti I/O QUAD SPI 1.70-1.95V 50M/104Mhz -40 to 125°C SOIC,USON Prod Multi I/O SPI, OPI, DTR 1.65-1.95V 50M/133Mhz -40 to 125°C SOIC, VVSOP, WSON, VSOP, Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC, WSON, USON, XSON, TFBGA Prod IBIS/Verilog IS25LP128F Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP128 IS25WP128F Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP128F Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP128F Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP128F Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP128F Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP128F Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP128F Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP128F Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP128F Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP128F Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP128F Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP128F Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP128F Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP128F Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP128F Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP128F Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA PROD IBIS/VERILO IS25LP128F MULTI I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA PROD IBIS/VERILO IS25LP128F MULTI I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -4 SOIC, WSON, TFBGA Prod IBIS/Verilog IS25WP128 256M IS25LP256E Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IBIS/Verilog IS25LP256D, IS25LP2 IBIS/Verilog IS25WP01G Multi I/O SPI, QPI, DTR 1.7-1.95V 50M/104Mhz -40 to 125°C LFBGA Prod IBIS/Verilog 2G IS25LP02GG Multi I/O SPI, QPI, DTR 2.7-3.6V 50M/133Mhz -40 to 105°C LFBGA Contact Factory IS25WP02GG Multi I/O SPI, QPI, DTR 1.65- 1.95V 50M/133Mhz -40 to 105°C LFBGA Contact ISSI to request SFDP table Den Part Number Buy Type Vcc Frequency Temp, Range Package Type Status Alt, Version/Doc 128M IS25LE128E Multi I/O SPI, OPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC.WSON.TFBGA Contact Factory 256M IS25LE256E Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE256E Multi I/O SPI, QPI, DTR 1.7-1.95V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M Multi I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA Prod IS25WE512M MULTI I/O SPI, QPI, DTR 2.3-3.6V 50M/133Mhz -40 to 125°C SOIC, WSON, TFBGA PROD IS25WE512M MULTI I/O SPI, QPI, DTR 2.3-3.6V 1.7-1.95V 50M/112Mhz -40 to 125°C SOIC, WSON, TFBGA Prod 1G IS25LE01G Multi I/O SPI, QPI, DTR 2.7-3.6V 50M/133Mhz -40 to 125°C LFBGA Prod IS25WE01G Multi I/O SPI, QPI, DTR 1.7-1.95V 50M/104Mhz -40 to 125°C LFBGA Prod Den Part Number Type Vcc Frequency Temp. Range Package Type Status Comment 64M IS25LX064 xSPI 2.7-3.6V 133Mhz -40 to 125°C SOIC, TFBGA S=NOW IS25WX064 xSPI 1.7-2.0V 200Mhz -40 to 125°C SOIC, TFBGA S=NOW IS25WX128 xSPI S=NOW IS25WX256 xSPI 1.7-2.0V 200Mhz -40 to 125°C SOIC, TFBGA S=NOW 512M IS25LX512M xSPI 2.7-3.6V 133Mhz -40 to 125°C SOIC, TFBGA S=NOW IS25WX512M xSPI 1.7-2.0V 200Mhz -40 to 125°C SOIC, TFBGA S=NOW IS25WX512M xSPI 1.7--40 to 125°C SOIC,TFBGA S=Q4/22 2G IS25LX02GA xSPI 2.7-3.6V 133Mhz -40 to 125°C TFBGA Contact Factory IS25WX02GA xSPI 1.7-2.0V 200Mhz -40 to 125°C TFBGA Contact Factory Den Part Number Buy Type Vcc Frequency Temp.Range Package Type Status Comment 256M IS25DLP256M Multi I/O SPI, QPI, DTR 2.3-3.6V 80M/166Mhz -40 to 125°C SOIC,TFBGA Contact Factory IS25DWP256M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP2512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.95V 80M/166Mhz -40 to 125°C SOIC,TFBGA Prod IS25DLP512M Multi I/O SPI, QPI, DTR 1.65-1.9 Contact Factory Den Part Number Buy Vcc Ecc Requirement Bus Width Sequential Read Speed (ns) Temp.Range Package Type Status 1G IS34ML01G084 3.3V 4-bit X8 25 -40°C to 105°C 48-TSOP, 63-BGA Prod 1G IS34ML01G084 3.3V 4-bit X8 25 -40°C to 105°C 48-TSOP, 63-BGA Prod 1G IS34ML01G084 3.3V 4-bit X8 25 -40°C to 105°C 48-TSOP, 63-BGA Prod 1G IS34ML01G084 3.3V 4-bit X8 25 -40°C to 105°C 48-TSOP, 63-BGA Prod 1G IS34ML01G084 3.3V 4-bit X8 25 -40°C to 105°C 48-TSOP, 63-BGA Prod 1G IS34ML01G084 3.3V 4-bit X8 25 -40°C to 105°C 48-TSOP, 63-BGA Prod 1G IS34ML01G084 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Simulation Models not listed above may be available upon request S = Sample, Prod = Production NR = Not Recommended for new designs EOL = End of Life IF YOU DON'T SEE A PRODUCT YOU ARE INTERESTED IN AND HAVE A SPECIAL REQUEST, CONTACT US AND LET US KNOW Integrated Silicon Solution, Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support applications where the life support applications where the life support applications whe Inc. receives written assurance to its satisfaction, that: a. the risk of injury or damage has been minimized; b. the user assume all such risks; and c. potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances Type of computer memory "PC100" redirects here. For the Japanese home computer, see NEC PC-100. Computer memory and data storage Direct-attached storage Network-attached storage Network-attach Storage area network Block-level storage Data Cluster Directory Shared resource File sharing File system Clustered file system Distributed file system Distributed file system for cloud Distributed data store Data tore Data tore Data tore Data tore Data store Distributed data store Data tore Data tore Data tore Distributed data store Data bank Data store Data bank Data store Data bank Data store Distributed data store Distributed data store Data tore Data tore Data bank Data store File deletion File copying Backup Core dump Hex dump Data communication Information transfer Temporary file Copy protection Digital rights management Volume boot record Disk array Disk image Disk mirroring Disk aggregation Disk partitioning Memory segmentation Locality of reference Logical disk Storage virtualization Virtual memory Memory-mapped file Software entropy Software rot In-memory database In-memory processing Persistent data structure RAID Non-RAID drive architectures Memory paging Bank switching Grid computing Cloud storage Fog computing Edge computing Dew computing Amdahl's law Moore's law Kryder's law Volatile RAM Hardware cache CPU cache Scratchpad memory DRAM eDRAM SDRAM DDR GDDR HBM SRAM 1T-SRAM ReRAM QRAM Content-addressable memory (CAM) VRAM Dual-ported RAM Video RAM (dual-ported DRAM) Historical Williams-Kilburn tube (1946-1947) Delay-line memory (1947) Mellon optical memory (1951) Selectron tube (1952) Dekatron T-RAM (2009) Z-RAM (2002-2010) Non-volatile ROM MROM PROM EPROM ROM cartridge Solid-state storage (SSS) Flash memory is used in: Solid-state drive (SSD) Solid-state hybrid drive (SSHD) USB flash drive IBM FlashSystem Flash Core Module Memory Card Memory Stick CompactFlash PC Card MultiMediaCard SD card SIM card Simony Stick CompactFlash PC Card MultiMediaCard SD card SIM card Simony Stick CompactFlash PC Card MultiMediaCard SD card SD card SD card CBRAM Early-stage NVRAM FeRAM ReRAM FeFET memory Analog recording Phonograph record Quadruplex videotape Vision Electronic Recording Apparatus Magnetic tape tape Linear Tape-Open Betamax 8 mm video format DV MiniDV MicroMV U-matic VHS S-VHS VHS-C D-VHS Hard disk drive Optical data storage Optical disc CD-ROM DVD DVD+R DVD-Video DVD card DVD-RAM MiniDVD HD DVD Blu-ray Ultra HD Blu-ray Holographic Versatile Disc WORM In development CBRAM Racetrack memory NRAM Millipede memory NRAM Millipede memory NRAM Millipede memory Time crystal Quantum memory UltraRAM Historical Paper data storage (1725) Punched card (1725) Punched tape (1725) Punched tape (1725) Plugboard Delay-line memory (1960s) Thin-film memory (1962) Disk pack (1962) Twistor memory (-1968) Bubble memory (-1970) Floppy disk (1971) vte SDRAM memory module Synchronous dynamic random-access memory (synchronous dynamic RAM or SDRAM) is any DRAM where the operation of its external pin interface is coordinated by an externally supplied clock signal. DRAM integrated circuits (ICs) produced from the early 1970s to early 1990s used an asynchronous interface, in which input control signals have a direct effect on internal functions only delayed by the trip across its semiconductor pathways. SDRAM has a synchronous internal functions only delayed by the trip across its semiconductor pathways. state machine that responds to incoming commands. These commands can be pipelined to improve performance, with previously started operations completing while new commands are received. The memory is divided into several equally sized but independent sections called banks, allowing the device to operate on a memory access command in each bank simultaneously and speed up access in an interleaved fashion. This allows SDRAMs to achieve greater concurrency and higher data transfer rates than asynchronous DRAMs could. Pipelining means that the chip can accept a new command before it has finished processing the previous one. For a pipelined write, the write command can be immediately followed by another command without waiting for the data to be written into the memory array. For a pipelined read, the requested data appears a fixed number of clock cycles (latency) after the read command, during which additional commands can be sent. History Eight Hyundai SDRAM ICs on a PC100 DIMM package The earliest DRAMs were often synchronous design, but in the 1990s returned to synchronous operation.[1][2] The first commercial SDRAM was the Samsung KM48SL2000 memory chip, which had a capacity of 16 Mbit.[3] It was manufactured by Samsung Electronics using a CMOS (complementary metal-oxide-semiconductor) fabrication process in 1992,[4] and mass-produced in 1993.[3] By 2000, SDRAM had replaced virtually all other types of DRAM in modern computers, because of its greater performance. asynchronous DRAM. Indeed, early SDRAM was somewhat slower than contemporaneous burst EDO DRAM due to the additional logic. The benefits of SDRAM's internal buffering come from its ability to interleave operations to multiple banks of memory, thereby increasing effective bandwidth. Today, virtually all SDRAM is manufactured in compliance with standards established by JEDEC, an electronics industry association that adopts open standards to facilitate interoperability of electronic components. JEDEC formally adopted its first SDRAM standards to facilitate interoperability of electronic components. SDRAM, known as DDR SDRAM, was first demonstrated by Samsung in 1997.[5] Samsung released the first commercial DDR SDRAM chip (64 Mbit[6]) in June 1998,[7][8][9] followed soon after by Hyundai Electronics (now SK Hynix) the same year.[10] SDRAM is also available in registered varieties, for systems that require greater scalability such as servers and workstations. Today, the world's largest manufacturers of SDRAM include: Samsung Electronics, SK Hynix, Micron Technology, and Nanya Technology, and Nanya Technology. for 100 MHz SDRAM (1 MHz = 10 6 {\displaystyle 10^{6}} Hz) to 5 ns for DDR-400, but has remained relatively unchanged through DDR2-800 and DDR3-1600 generations. However, by operating the interface circuitry at increasingly higher multiples of the fundamental read rate, the achievable bandwidth has increased rapidly. Another limit is the CAS latency, the time between supplying a column address and receiving the corresponding data. Again, this has remained relatively constant at 10-15 ns through the last few generations of DDR SDRAM. In operation, CAS latency is a specific number of clock cycles programmed into the SDRAM's mode register and expected by the DRAM controller. Any value may be programmed, but the SDRAM will not operate correctly if it is too low. At higher clock rates, the useful CAS latency in clock of DDR-400 SDRAM, CL4-6 for DDR2-800, and CL8-12 for DDR3-1600. Slower clock cycles will naturally allow lower numbers of CAS latency cycles. SDRAM modules have their own timing specifications, which may be slower than those of the chips on the module. When 100 MHz modules that could not reliably operate at that clock rate. In response, Intel published the PC100 standard, which outlines requirements and guidelines for producing a memory module that can operate reliably at 100 MHz. This standard was widely influential, and the term "PC100" guickly became a common identifier for 100 MHz SDRAM modules, and modules are now commonly designated with "PC"-prefixed numbers (PC66, PC100 or PC133 - although the actual meaning of the numbers has changed). Control signals All commands are timed relative to the rising edge of a clock signal. In addition to the clock, there are six control signals, mostly active low, which are sampled on the rising edge of the clock signal. are interpreted and command latency times do not elapse. The state of other control lines is not relevant. The effect of this signal is actually delayed by one clock cycle is ignored, except for testing the CKE input again. Normal operations resume on the rising edge of the clock after the one where CKE is sampled high. Put another way, all other chip operations are timed relative to the rising edge of a masked clock. The masked clock. The masked clock is the logical AND of the input clock and the state of the chip ignores all other inputs (except for CKE), and acts as if a NOP command is received. DQM data mask. (The letter Q appears because, following digital logic conventions, the data is not actually written to the DRAM. When asserted high two cycles before a read cycle, the read data is not output from the chip. There is one DQM line per 8 bits on a x16 memory chip or DIMM. Command bit. Along with CAS and WE, this selects one of eight commands. CAS, column address strobe. This is also not a strobe, rather a command bit. Along with RAS and WE, this selects one of eight commands. WE, write enable. Along with RAS and CAS, this selects one of eight commands. It generally distinguishes read-like commands. It generally distinguishes read-like commands. It generally distinguishes read-like commands. WE, write enable. internal data banks. One to three bank address inputs (BA0, BA1 and BA2) are used to select which bank a command is directed toward. Address input pins. Some commands, which either do not use an address, or present a column address, also use A10 to select variants. Commands The SDR SDRAM commands are defined as follows: CS RAS CAS WE BAn A10 An Command H x x x x x Command inhibit (no operation) L H H H x x x No operation) L H H H x x x X No operation L H H L x x x Burst terminate: stop a burst read or burst write in progress L H L H bank H column Read with auto precharge: as above, and precharge (close row) when done L H L bank L column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently active row L H L L bank H column Write: write a burst of data to the currently activ bank L x Precharge: deactivate (close) the current row of selected bank L L H L x H x Precharge all: deactivate (close) the current row of all banks must be precharged. L L L U 0 0 mode Load mode register: A0 through A9 are loaded to configure the DRAM chip.The most significant settings are CAS latency (2 or 3 cycles) and burst length (1, 2, 4 or 8 cycles) All SDRAM generations (SDR and DDRx) use essentially the same commands, with the changes being: Additional address bits to support larger devices Additional bank select bits Wider mode registers (DDR2 and up use 13 bits, A0-A12) Additional extended mode registers (selected by the bank address bits) DDR2 deletes the burst terminate command; DDR3 reassigns it as "ZQ calibration" DDR3 and DDR4 use A12 during which the other control lines are used as row address bits 16, 15 and 14. When ACT is high, other commands are the same as above. Construction and operation SDRAM DIMM (which contains 512 MB), might be made of eight or nine SDRAM chips, each containing 512 Mbit of storage, and each one contributing 8 bits to the DIMM's 64- or 72-bit width. A typical 512 Mbit SDRAM chip internally contains four independent 16 MB memory banks. Each bank is either idle, active, or changing from one to the other.[6] The active command activates an idle bank. It presents a two-bit bank address (BA0-BA1) and a 13-bit row address (A0-A12), and causes a read of that row into the bank's array of all 16,384 column sense amplifiers. This is also known as "opening" the row. This operation has the side effect of refreshing the dynamic (capacitive) memory storage cells of that row. Once the row has been activated or "opened", read and write commands are possible to that row. Activation requires a minimum amount of time, called the row-to-column delay, or tRCD before reads or writes to it may occur. This time, rounded up to the next multiple of the clock period, specifies the minimum number of wait cycles between an active command, and a read or write command. During these wait cycles, additional commands may be sent to other banks; because each bank operates completely independently. Both read and write commands require a column address each bank operates completely independently. Both read and write commands require a column address lines (A0-A9, A11). When a read command is issued, the SDRAM will produce the corresponding output data on the DQ lines in time for the rising edge of the clock a few clock cycles later, depending on the configured CAS latency. Subsequent words of the burst will be produced in time for subsequent words of the burst will be produced in time for the rising edge of the clock a few clock be written driven on to the DQ lines during the same rising clock edge. It is the duty of the memory controller to ensure that it needs to drive write data on to those lines. This can be done by waiting until a read burst, or by using the DQM control line. When the memory controller needs to access a different row, it must first return that bank's sense amplifiers to an idle state, ready to sense the next row. This is known as a "precharge" operation, or "closing" the row. A precharge may be commanded explicitly, or it may be performed automatically at the conclusion of a read or write operation. Again, there is a minimum time, the row precharge delay, tRP, which must elapse before that row is fully "closed" and so the bank. Although refreshing a row is an automatic side effect of activating it, there is a minimum time for this to happen, which requires a minimum row access time tRAS delay between an active command opening a row, and the corresponding precharge command closing it. This limit is usually dwarfed by desired read and write commands to the row, so its value has little effect on typical performance. Command interactions The no operation command is always permitted, while the load mode register command requires that all banks be idle, and a delay afterward for the changes to take effect. The auto refresh cycle time tRFC to return the chip to the idle state. (This time is usually equal to tRCD+tRP.) The only other command that is permitted on an idle bank is the active command. This takes, as mentioned above, tRCD before the row is fully open and can accept read and write commands. When a bank is open, there are four commands. When a bank is open, there are four commands. When a bank is open, there are four commands. A read, burst terminate, or precharge command may be issued on cycle 0, another read command is issued on cycle 0, another read command is issued on cycle 3, then the first read command will begin bursting data out during cycles 3 and 4, then the results from the second read command will appear beginning with cycle 5. If the command issued on cycle 5. Although the interrupting read may be to any active bank, a precharge command will only interrupt the read burst if it is to the same bank or all banks; a precharge command to a different bank will not interrupt a read burst. Interrupting a read burst by a write command is possible, but more difficult. It can be done if the DQM signal is used to suppress output from the SDRAM in time for the write operation. Because the effects of DQM on read data are delayed by two cycles, but the effects of DQM on write data are immediate, DQM must be raised (to mask the read data) beginning at least two cycles before write command but must be lowered for the cycle of the write command is intended to have an effect). Doing this in only two clock cycles requires careful coordination between the time the SDRAM for the write on the following clock edge. If the clock frequency is too high to allow sufficient time, three cycles may be required. If the read command includes auto-precharge, the precharge begins the same cycle as the interrupting command. Burst ordering A modern microprocessor with a cache line requires eight consecutive accesses to a 64-bit DIMM, which can all be triggered by a single read or write command by configuring the SDRAM chips, using the mode register, to perform eight-word bursts. A cache line fetch is typically triggered by a read from a particular address, and SDRAM chips or DIMM, which is 64 bits for a typical DIMM.) SDRAM chips support two possible conventions for the ordering of the remaining words in the cache line. Bursts always access an aligned block of BL consecutive words beginning on a multiple of BL. So, for example, a four-word burst access to any column address from four to seven. The ordering, however,

depends on the requested address, and the configured burst type option: sequential or interleaved. Typically, a memory controller will requested word is the only word accessed. For a burst length of two, the requested word is the only word accessed. For a burst length of two, the requested word is the only word accessed. accessed first, and the other word in the aligned block is accessed second. This is the following word if an even address was specified, and the previous word if an odd address was specified. For the sequential burst mode, later words are accessed in increasing address was specified. example, for a burst length of four, and a requested column address of five, the words would be accessed in the order 5-6-7-4. If the burst length, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length of four, and a requested column address of five, the words would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the burst length were eight, the access order would be 5-6-7-4. If the access order would be access order would be access order wo using an exclusive or operation between the counter and the address. Using the same starting address of five, a four-word burst would be 5-4-7-6. An eight-word burst would be 5-4-7-6. An eight-word burst would be 5-4-7-6. [citation needed] If the requested column address is at the start of a block, both burst modes (sequential and interleaved) return data in the same sequential and interleaved) return data in the same sequential and interleaved) return data in the same sequential sequence 0-1-2-3-4-5-6-7. The difference only matters if fetching a cache line from memory in critical-word-first order. Mode register Single data rate SDRAM has a single 10-bit programmable mode register. Later double-data-rate SDRAM standards add additional mode registers, address pins. For SDR SDRAM, the bank address pins and address pins and address pins. For SDR SDRAM, the bank address pins and address pins. mode register cycle. M9: Write burst mode. If 0, writes use the read burst length and mode. If 1, all writes are non-burst (single location). M8, M7: Operating mode. Reserved, and must be 00. M6, M5, M4: CAS latency. Generally only 010 (CL2) and 011 (CL3) are legal. Specifies the number of cycles between a read command and data output from the chip. The chip has a fundamental limit on this value in nanoseconds; during initialization, the memory controller must use its knowledge of the clock frequency to translate that limit into cycles. M3: Burst type. 0 - requests sequential burst ordering, while 1 requests interleaved burst ordering. M2, M1, M0: Burst length. Values of 000, 001, 010 and 011 specify a burst size of 1, 2, 4 or 8 words, respectively. Each read (and write, if M9 is 0) will perform that many accesses, unless interrupted by a burst stop or other command. A value of 111 specifies a full-row burst. The burst will continue until interrupted by a burst stop or other command. A value of 11 specifies a full-row burst stop or other command. SDRAM standards use more mode register bits, and provide additional mode registers. The register command. For example, DDR2 SDRAM has a 13-bit mode register value mode register No. 1 (EMR1), and a 5-bit extended mode register No. 2 (EMR2). Auto refresh It is possible to refresh a RAM chip by opening and closing (activating and precharging) each row in each bank. However, to simplify the memory controller, SDRAM also maintains an internal counter, which iterates over all possible rows. The memory controller must simply issue a sufficient number of auto refresh interval (tREF = 64 ms is a common value). All banks must be idle (closed, precharged) when this command is issued. Low power modes As mentioned, the clock enable (CKE) input can be used to effectively stop the clock to an SDRAM. The CKE input is sampled each rising edge of the clock is ignored for all purposes other than checking CKE. As long as CKE is low, it is permissible to change the clock rate, or even stop the clock entirely. If CKE is lowered while the SDRAM is performing operations, it simply "freezes" in place until CKE is raised again. If the SDRAM automatically enters power-down mode, consuming minimal power until CKE is raised again. This must not last longer than the maximum refresh interval tREF, or memory contents may be lost. It is legal to stop the clock entirely during this time for additional power savings. Finally, if CKE is lowered at the same time as an auto-refresh command is sent to the SDRAM, the SDRAM enters self-refresh mode. to generate internal refresh cycles as necessary. The clock may be stopped during this time. While self-refresh mode consumes slightly more power than makes up the difference. SDRAM designed for battery-powered devices offers some additional power-saving options. One is temperature-dependent refresh; an on-chip temperature sensor reduces the refresh to a portion of the DRAM array. The fraction which is refreshed is configured using an extended mode register. The third, implemented in Mobile DDR (LPDDR) and LPDDR2 is "deep power down" mode, which invalidates the memory and requires a full reinitialization to exit from. This is activated by sending a "burst terminate" command while lowering CKE. DDR SDRAM prefetch architecture DDR SDRAM employs prefetch architecture to allow quick and easy access to multiple data words located on a common physical row in the memory. The prefetch architecture takes advantage of the specific characteristics of memory access to DRAM. Typical DRAM memory operation, as it involves the careful sensing of the tiny signals in DRAM memory cells; it is the slowest phase of memory operation. However, once a row is read, subsequent column accesses to that same row can be very quick, as the sense amplifiers also act as latches. For reference, a row of a 1 Gbit[6] DDR3 device is 2,048 bits wide, so internally 2,048 bits are read into 2,048 separate sense amplifiers during the row access phase. Row accesses might take 50 ns, depending on the speed of the DRAM, whereas column access to bits on an open row. For an 8-bit-wide memory chip with a 2,048 bit wide row, accesses to any of the 256 datawords (2048/8) on the row can be very quick, provided no intervening accesses to other rows occur. The drawback of the older fast column address had to be sent for each additional dataword on the row. The address bus had to operate at the same frequency as the data bus. Prefetch architecture simplifies this process by allowing a single address request to result in multiple data words. In a prefetch buffer architecture, when a memory access occurs to a row the buffer grabs a set of adjacent data words. In a prefetch buffer architecture, when a memory access occurs to a row the need for individual column address requests. This assumes the CPU wants adjacent data words in memory, which in practice is very often the case. For instance, in DDR1, two adjacent data words will be read from each chip in the same clock cycle and placed in the pre-fetch buffer. Each word will then be transmitted on consecutive rising and falling edges of the clock cycle. Similarly, in DDR2 with a 4n pre-fetch buffer, four consecutive data words are read and placed in buffer while a clock, which is twice faster than the internal clock [12] The prefetch buffer depth can also be thought of as the ratio between the core memory frequency and the IO frequency. In an 8n prefetch architecture (such as DDR3), the IOs will operate 8 times faster (1600 megabits per second). If the memory has 16 IOs, the total read bandwidth would be 200 MHz x 8 datawords/access x 16 IOs = 25.6 gigabits per second (Gb/s). Modules with multiple DRAM chips can provide correspondingly higher bandwidth. Each generation of SDRAM has a different prefetch buffer size: DDR SDRAM's prefetch buffer size: size is 2n (two datawords per memory access) DDR2 SDRAM's prefetch buffer size is 8n (eight datawords per memory access) DDR3 SDRAM's prefetch buffer size is 8n; there is an additional mode 16n Generations SDRAM feature map Type Feature changes SDRAM Vcc = 2.5 V2.5 - 7.5 ns per cycle Signal: LVTTL DDR1 Access is ≥ 4 words "Burst terminate" removed 4 units used in parallel 1.25 - 5 ns per cycle Signal: SSTL 2 (2.5V)[13] DDR2 Access is ≥ 4 words "Burst terminate" removed 4 units used in parallel 1.25 - 5 ns per cycle Signal: SSTL 2 (2.5V)[13] DDR2 Access is ≥ 4 words "Burst terminate" removed 4 units used in parallel 1.25 - 5 ns per cycle Signal: SSTL 2 (2.5V)[13] DDR2 Access is ≥ 4 words "Burst terminate" removed 4 units used in parallel 1.25 - 5 ns per cycle Signal: SSTL 2 (2.5V)[13] DDR2 Access is ≥ 4 words "Burst terminate" removed 4 units used in parallel 1.25 - 5 ns per cycle Signal: SSTL 2 (2.5V)[13] DDR2 Access is ≥ 4 words "Burst terminate" removed 4 units used in parallel 1.25 - 5 ns per cycle Signal: SSTL 2 (2.5V)[13] DDR2 Access is ≥ 4 words "Burst terminate" removed 4 units used in parallel 1.25 - 5 ns per cycle Signal: SSTL 2 (2.5V)[13] DDR2 Access is ≥ 4 words "Burst terminate" removed 4 units used in parallel 1.25 - 5 ns per cycle Signal: SSTL 2 (2.5V)[13] DDR2 Access is ≥ 4 words "Burst terminate" removed 4 units used in parallel 1.25 - 5 ns per cycle Signal: SSTL 2 (2.5V)[13] DDR2 Access is ≥ 4 words "Burst terminate" removed 4 units used in parallel 1.25 - 5 ns per cycle Signal: SSTL 2 (2.5V)[13] DDR2 Access is ≥ 4 words "Burst terminate" removed 4 units used in parallel 1.25 - 5 ns per cycle Signal: SSTL 2 (2.5V)[13] DDR2 Access is ≥ 4 words "Burst terminate" removed 4 units used in parallel 1.25 - 5 ns per cycle Signal: SSTL 2 (2.5V)[13] DDR2 Access is ≥ 4 words "Burst terminate" removed 4 units used in parallel 1.25 - 5 ns per cycle Signal: SSTL 2 (2.5V)[13] DDR2 Access is ≥ 4 words "Burst terminate" removed 4 units used in parallel 1.25 - 5 ns per cycle Signal: SSTL 2 (2.5V)[13] DDR2 Access is ≥ 4 words "Burst terminate" removed 4 units used in parallel 1.25 - 5 ns per cycle Signal: SSTL 2 (2.5V)[13] DDR2 Access is ≥ 4 words "Burst termi SSTL 18 (1.8V)[13] DDR3 Access is ≥8 words Signal: SSTL 15 (1.5V)[13] Much longer CAS latencies DDR4 Vcc ≤ 1.2 V point-to-point (single module per channel) SDR The 64 MB[6] of sound memory on the Sound Blaster X-Fi Fatality Pro sound card is built from two Micron 48LC32M8A2 SDRAM chips. They run at 133 MHz (7.5 ns clock period) and have 8-bit wide data buses.[14] Originally simply known as SDRAM, single data rate SDRAM, single data rate SDRAM can accept one word of data per clock cycle. Chips are generally assembled into 168-pin DIMMs that read or write 64 (non-ECC) or 72 (ECC) bits at a time. Use of the data bus is intricate and thus requires a complex DRAM controller circuit. This is because data written to the DRAM must be presented in the same cycle as the write command, but reads produce output 2 or 3 cycles after the read command. The DRAM controller must ensure that the data bus is never required for a read and a write at the same time. Typical SDR SDRAM clock rates are 66, 100, and 133 MHz (periods of 15, 10, and 7.5 ns), respectively denoted PC66, PC100, and PC133. Clock rates up to 200 MHz were available. It operates at a voltage of 3.3 V. This type of SDRAM is slower than the DDR variants, because only one word of data is transmitted per clock cycle (single data rate). But this type is also faster than its predecessors extended data out DRAM (EDO-RAM) and fast page mode DRAM (FPM-RAM) which took typically two or three clocks to transfer one word of data. PC66 PC66 refers to internal removable computer memory standard defined by the JEDEC. PC66 is Synchronous DRAM operating at a clock frequency of 66.66 MHz, on a 64-bit bus, at a voltage of 3.3 V. PC66 is available in 168-pin DIMM and 144-pin SO-DIMM form factors. The theoretical bandwidth is 533 MB/s. (1 MB/s = one million bytes per second) This standard was used by Intel Pentium and AMD K6-based PCs. It also features in the Beige Power Mac G3, early iBooks and PowerBook G3s. It is also used in many early Intel Celeron systems with a 66 MHz FSB. It was superseded by the PC100 and PC133 standards. PC100 refers. PC10 to Synchronous DRAM operating at a clock frequency of 100 MHz, on a 64-bit-wide bus, at a voltage of 3.3 V. PC100 is available in 168-pin DIMM and 144-pin SO-DIMM form factors. PC100 is backward compatible with PC66 and was superseded by the PC133 standard. A module built out of 100 MHz SDRAM chips is not necessarily capable of operating at 100 MHz. The PC100 standard specifies the capabilities of the memory module as a whole. PC100 is used in many older computers; PCs around the late 1990s were the most common computers; PCs around the late 1990s were the most common computers with PC100 memory. frequency of 133 MHz, on a 64-bit-wide bus, at a voltage of 3.3 V. PC133 is available in 168-pin DIMM and 144-pin SO-DIMM form factors. PC133 is the fastest and final SDR SDRAM standard ever approved by the JEDEC, and delivers a bandwidth of 1.066 GB per second ([133.33 MHz * 64/8]=1.066 GB/s). (1 GB/s = one billion bytes per second) PC133 is backward compatible with PC100 and PC66. DDR Main article: DDR SDRAM While the access latency of DRAM is fundamentally limited by the DRAM array, DRAM has very high potential bandwidth because each internal read is actually a row of many thousands of bits. To make more of this bandwidth available to users, a double data rate interface was developed. This uses the same commands, accepted once per cycle, but reads or writes two words of data per clock cycle. The DDR interface accomplishes this by reading and writing data on both the rising and falling edges of the clock signal. In addition, some minor changes to the SDR interface timing were made in hindsight, and the supply voltage was reduced from 3.3 to 2.5 V. As a result, DDR SDRAM is not backwards compatible with SDR SDRAM. DDR SDRAM (sometimes called DDR1 for greater clarity) doubles the minimum read or write unit; every access refers to at least two consecutive words. Typical DDR SDRAM is not backwards compatible with SDR SDRAM. DDR SDRAM (sometimes called DDR1 for greater clarity) doubles the minimum read or write unit; every access refers to at least two consecutive words. Typical DDR SDRAM is not backwards compatible with SDR SDRAM. ns/cycle), generally described as DDR-266, DDR-333 and DDR-400 (3.75, 3, and 2.5 ns per beat). Corresponding 184-pin DIMMs are known as PC-2100, PC-2700 and PC-3200. Performance up to DDR-550 (PC-4400) is available. DDR2 Main article: DDR2 SDRAM is very similar to DDR SDRAM, but doubles the minimum read or write unit again, to four consecutive words. The bus protocol was also simplified to allow higher performance operations; instead, internal RAM operations; instead, internal operations are performed in units four times as wide as SDRAM. Also, an extra bank address pin (BA2) was added to allow eight banks on large RAM chips. Typical DDR2 SDRAM clock rates are 200, 266, 333 or 400 MHz (periods of 5, 3.75, 3 and 2.5 ns), generally described as DDR2-400, DDR2-533, DDR2-667 and DDR2-800 (periods of 5, 3.75, 1.5 and 1.25 ns). Corresponding 240-pin DIMMs are known as PC2-3200 through PC2-6400. DDR2 SDRAM is now available at a clock rate of 533 MHz generally described as DDR2-1066 and the corresponding DIMMs are known as PC2-8600 depending on the manufacturer). Performance up to DDR2-1250 (PC2-10000) is available. Note that because internal operations are at 1/2 the clock rate 200 MHz). DDR3 Main article: DDR3 SDRAM DDR3 continues the trend, doubling the minimum read or write unit to eight consecutive words. This allows another doubling of bandwidth and external bus rate without having to change the clock rate of internal operations, just the width. To maintain 800-1600 M transfers/s (both edges of a 400-800 MHz clock), the internal RAM array has to perform 100-200 M fetches per second. Again, with every doubling, the downside is the increased latency. As with all DDR SDRAM generations, commands are still restricted to one clock edge and command latencies are given in terms of clock cycles, which are half the speed of the usually quoted transfer rate (a CAS latency of 8 with DDR3-800 is 8/(400 MHz) = 20 ns, exactly the same latency of CAS2 on PC100 SDR SDRAM). DDR3 memory chips are being made commercially,[15] and computer systems using them were available from the second half of 2007,[16] with significant usage from 2008 onwards.[17] Initial clock rates were 400 and PC3-8500 modules), but 667 and 800 MHz, described as DDR3-1060 (PC3-10600 and PC3-12800 modules) are now common.[18] Performance up to DDR3-2800 (PC3 22400 modules) are available.[19] DDR4 Main article: DDR4 SDRAM is the successor to DDR3 SDRAM. It was revealed at the Intel Developer Forum in San Francisco in 2008, and was due to be released to market during 2011. The timing varied considerably during its development - it was originally expected to be released in 2012,[20] and later (during 2010) expected to be released in 2015,[21] before samples were announced in early 2011 and manufacturers began to announce that commercial production and release to market was anticipated in 2012. DDR4 reached mass market adoption around 2015, which is comparable with the approximately five years taken for DDR3 to achieve mass market transition over DDR2. The DDR4 chips run at 1.2 V or less, [22][23] compared to the 1.5 V of DDR3 chips, and have in excess of 2 billion data transfers per second. They were expected to be introduced at frequency rates of 2133 MHz, estimated to rise to a potential 4266 MHz[24] and lowered voltage of 1.05 V[25] by 2013. DDR4 did not double the internal prefetch width again, but uses the same 8n prefetch as DDR3.[26] Thus, it will be necessary to interleave reads from several banks to keep the data bus busy. In February 2009, Samsung validated 40 nm DRAM chips, considered a "significant step" towards DDR4 did not double the internal prefetch width again, but uses the same 8n prefetch as DDR4.[26] Thus, it will be necessary to interleave reads from several banks to keep the data bus busy. In February 2009, Samsung validated 40 nm DRAM chips, considered a "significant step" towards DDR4.[26] Thus, it will be necessary to interleave reads from several banks to keep the data bus busy. In February 2009, Samsung validated 40 nm DRAM chips, considered a "significant step" towards DDR4.[26] Thus, it will be necessary to interleave reads from several banks to keep the data bus busy. In February 2009, Samsung validated 40 nm DRAM chips, considered a "significant step" towards DDR4.[26] Thus, it will be necessary to interleave reads from several banks to keep the data bus busy. In February 2009, Samsung validated 40 nm DRAM chips, considered a "significant step" towards DDR4.[26] Thus, it will be necessary to interleave reads from several banks to keep the data bus busy. In February 2009, Samsung validated 40 nm DRAM chips, considered a "significant step" towards DDR4.[26] Thus, it will be necessary to interleave reads from several banks to keep the data bus busy. In February 2009, Samsung validated 40 nm DRAM chips, considered a "significant step" towards DDR4.[26] Thus, it will be necessary to interleave reads from several banks to keep the data bus busy. In February 2009, Samsung validated 40 nm DRAM chips, considered a "significant step" towards DDR4.[26] Thus, it will be necessary to interleave reads from several banks to keep the data bas busy. In February 2009, Samsung validated 40 nm DRAM chips, considered a "significant step" towards DDR4.[26] Thus, it will be necessary to interleave rea development[27] since, as of 2009, current DRAM chips were only beginning to migrate to a 50 nm process.[28] In January 2011, Samsung announced the completion and release for testing of a 30 nm 2048 MB[6] DDR4 DRAM module. It has a maximum bandwidth of 2.13 Gbit/s at 1.2 V, uses pseudo open drain technology and draws 40% less power than an equivalent DDR3 module.[29][30] DDR5 Main article: DDR5 SDRAM In March 2017, JEDEC announced a DDR5 standard is under development,[31] but provided no details except for the goals of doubling the bandwidth of DDR4, reducing power consumption, and publishing the standard was released on 14 July 2020. [32] Failed successors In addition to DDR, there were several other proposed memory technologies to succeed SDR SDRAM. Rambus DDR's to succeed SDR SDRAM. Rambus DDR's to succeed SDR SDRAM. 64 bit channel) caused it to lose the race to succeed SDR DRAM. Synchronous-link DRAM (SLDRAM) boasted higher performance and competed against RDRAM. It was developed during the late 1990s by the SLDRAM Consortium. The SLDRAM Consortium consisted of about 20 major DRAM and computer industry manufacturers. (The SLDRAM Consortium became incorporated as SLDRAM Inc. and then changed its name to Advanced Memory International, Inc.). SLDRAM was an open standard and did not require licensing fees. The specifications called for a 64-bit bus running at a 200, 300 or 400 MHz clock frequency. This is achieved by all signals being on the same line and thereby avoiding the synchronization time of multiple lines. Like DDR SDRAM, SLDRAM uses a double-pumped bus, giving it an effective speed of 400,[33] 600,[34] or 800 MT/s. (1 MT/s = 1000^2 transfers per second) SLDRAM used an 11-bit command bus (10 command bus (10 command bits CA9:0 plus one start-of-command FLAG line) to transmit 40-bit command packets on 4 consecutive edges of a differential command clock (CCLK/CCLK#). Unlike SDRAM, there were no per-chip select signals; each chip was assigned an ID when reset, and the command contained the ID of the chip that should process it. Data was transferred in 4- or 8-word bursts across an 18-bit (per chip) data bus, using one of two differential data clocks (DCLK0/DCLK0# and DCLK1/DCLK1#). Unlike standard SDRAM, the clock was generated by the data source (the SLDRAM chip in the case of a read operation) and transmitted in the same direction as the data, greatly reducing data skew. To avoid the need for a pause when the source of the DCLK changes, each command specified which DCLK pair it would use.[35] The basic read/write command consisted of (beginning with CA9 of the first word): SLDRAM Read, write or row op request packet FLAG CA9 CA8 CA7 CA6 CA5 CA4 CA3 CA2 CA1 CA0 1 ID8 Device ID ID CMD5 0 Command code CMD0 Bank Row 0 Row (continued) 0 0 0 0 0 0 Column 9 bits of device ID 6 bits of command 3 bits of bank address 10 or 11 bits of row address 5 or 4 bits spare for row or column expansion 7 bits of column address multiple devices. Any aligned power-of-2 sized group could be addressed. If the transmitted msbit was set, all leastsignificant bits up to and including the least-significant 0 bit of the transmitted address matching becomes a special case of this pattern.) A read/write command had the msbit clear: CMD5=0 CMD4=1 to open (activate) the specified row; CMD4=0 to use the currently open row CMD3=1 to transfer an 8-word burst; CMD3=0 for a 4-word burst; CMD1=0 to leave it open CMD0 selects the DCLK1 or DCLK0) A notable omission from the specification was per-byte write enables; it was designed for systems with caches and ECC memory, which always write in multiples of a cache line. Additional commands (with CMD5 set) opened and closed rows without a data transfer, performed refresh operations, read or wrote configuration registers, and performed other maintenance operations. Most of these commands supported an additional 4-bit sub-ID (sent as 5 bits, using the same multiple-destination encoding as the primary ID) which could be used to distinguish devices that were assigned the same multiple-destination encoding as the primary ID because they were connected in parallel and always read/written at the same multiple-destination encoding as the primary ID because they were a number of 8-bit control registers and 32-bit sub-ID (sent as 5 bits, using the same multiple-destination encoding as the primary ID because they were connected in parallel and always read/written at the same multiple-destination encoding as the primary ID because they were a number of 8-bit control registers and 32-bit sub-ID (sent as 5 bits, using the same multiple-destination encoding as the primary ID because they were a number of 8-bit control registers and 32-bit sub-ID (sent as 5 bits, using the same multiple-destination encoding as the primary ID because they were a number of 8-bit control registers and 32-bit sub-ID (sent as 5 bits, using the same multiple-destination encoding as the primary ID because they were a number of 8-bit control registers and 32-bit sub-ID (sent as 5 bits, using the same multiple-destination encoding as the primary ID because they were a number of 8-bit control registers and 32-bit sub-ID (sent as 5 bits, using the same multiple-destination encoding as the primary ID because they were a number of 8-bit sub-ID (sent as 5 bits, using the same multiple-destination encoding as the primary ID (sent as 5 bits, using the same multiple-destination encoding as the primary ID (sent as 5 bits, using the same multiple-destination encoding as the primary ID (sent as 5 bits, using the same multiple-destination encoding as the primary ID (sent as 5 bits, using the same multiple-destination encoding as the primary ID (sent as 5 bits, using the same multiple-destination encoding as the primary ID (sent as 5 bits, using the same multiple-destination encoding as the primary ID (sent as 5 bits, using the same multi bit status registers to control various device timing parameters. Virtual channel memory (VCM) SDRAM that was a proprietary type of SDRAM that was designed by NEC, but released as an open standard with no licensing fees. It is pin-compatible with standard SDRAM, but the commands are different. The technology was a potential competitor of RDRAM because VCM was not nearly as expensive as RDRAM was. A Virtual Channel Memory (VCM) module is mechanically and electrically compatible with standard SDRAM, so support for both depends only on the capabilities of the memory controller. In the late 1990s, a number of PC northbridge chipsets (such as the popular VIA KX133 and KT133) included VCSDRAM support. VCM inserts an SRAM cache of 16 "channel" buffers, each 1/4 row "segment" in size, between DRAM banks' sense amplifier rows and the data I/O pins. "Prefetch" and "restore" commands, unique to VCSDRAM, copy data between the DRAM's sense amplifier rows and the data I/O pins. "Prefetch" and "restore" commands, unique to VCSDRAM, copy data between the DRAM's sense amplifier rows and the data I/O pins. SDRAM's read and write commands specify a channel number to access. Reads and writes may thus be performed independent of the currently active state of the DRAM array, with the equivalent of four full DRAM rows being "open" for access at a time. This is an improvement over the two open rows possible in a standard two-bank SDRAM. (There is actually a 17th "dummy channel" used for some operations.) To read from VCSDRAM, after the active command is required to copy data from the sense amplifier array to the channel number. Once this is performed, the DRAM array may be precharged while read commands to the channel buffer continue. To write, first the data is written to a channel buffer (typically previous initialized using a Prefetch command), then a restore command, with the same parameters as the prefetch command, with the same parameters as the prefetch command), then a restore command, with the same parameters as the prefetch command, with the same parameters as sense amplifier array. Unlike a normal SDRAM write, which must be performed to an active (open) row, the VCSDRAM bank must be precharged (closed) when the restore command is issued. An active command is issued. An active command is issued at the vertice to the DRAM array. There is, in addition, a 17th "dummy channel" which allows writes to the currently open row. It may not be read from, but may be prefetched to, written to, and restored to the same memory address as it was prefetched from, the channel buffers may also be used for very efficient copying or clearing of large, aligned memory blocks. (The use of quarter-row segments is driven by the fact that DRAM cells are narrower than SRAM cells. The SRAM bits they straddle.) Additional commands prefetch a pair of segments to a pair of channels, and an optional command combines prefetch, read, and precharge to reduce the overhead of random reads. The above are the [EDEC-standardized commands. Earlier chips did not support the dummy channel or pair prefetch, and use a different encoding for precharge. A 13-bit address bus, as illustrated here, is suitable for a device up to 128 Mbit[6]. It has two banks, each containing 8,192 rows and 8,192 columns. Thus, row addresses are 13 bits, segment addresses are two bits, and eight column addresses are 13 bits, segment. Synchronous Graphics RAM (SGRAM) is a specialized form of SDRAM for graphics adaptors. It is designed for graphics-related tasks such as texture memory and framebuffers, found on video cards. It adds functions such as bit masking (writing to a specified bit plane without affecting the others) and block write (filling a block of memory with a single colour). Unlike VRAM and WRAM, SGRAM is single-ported. However, it can open two memory pages at once, which simulates the dual-port nature of other video RAM technologies. The earliest known SGRAM memory are 8 Mbit[6] chips dating back to 1994; [38] and the NEC µPD481850, introduced in December 1994, [39] The earliest known commercial device to use SGRAM is Sony's PlayStation (PS) video game console, starting with the Japanese SCPH-5000 model released in December 1995, using the NEC µPD481850 chip.[40][41] Graphics double data rate SDRAM (GDDR SDRAM) Main article: GDDR SDRAM) Main article: GDDR SDRAM) Main article: GDDR SDRAM (GDDR SDRAM) Main article: GDDR SDRAM) Main article: GDDR SDRAM (GDDR SDRAM) Main article: GDDR SDRAM) Main article: GDDR SDRAM (GDDR SDRAM) Main article: GDDR SDRAM) Main article: GDDR SDRAM (GDDR SDRAM) Main article: GDDR SDRAM) Main article: GDDR SDRAM (GDDR SDRAM) Main article: GDDR SDRAM) Main article: GDDR SDRAM (GDDR SDRAM) Main article: GDDR SDRAM) Main article: GDDR SDRAM (GDDR SDRAM) Main article: GDDR SDRAM) Main article: GDDR SDRAM (GDDR SDRAM) Main article: GDDR SDRAM) Main article: GDDR SDRAM (GDDR SDRAM) Main article: GDDR SDRAM) Main article: GDDR SDRAM (GDDR SDRAM) Main article: GDDR SDRAM) Main article: GDDR SDRAM (GDDR SDRAM) MAIN designed to be used as the main memory of graphics processing units (GPUs). GDDR SDRAM is distinct from commodity types of DDR SDRAM such as DDR3, although they share some core technologies. Their primary characteristics are higher clock frequencies for both the DRAM core and I/O interface, which provides greater memory bandwidth for GPUs. As of 2018, there are six successive generations of GDDR; GDDR3, GDDR4, GDDR5, and GDDR5, GDDR4, GDDR5, and GDDR5X, GDDR6. GDDR was initially known as DDR SGRAM. It was commercially introduced as a 16 Mbit[6] memory chip by Samsung Electronics in 1998.[8] High Bandwidth Memory (HBM) Main article: High Bandwidth Memory High Bandwidth Memory (HBM) is a high-performance RAM interface for 3D-stacked SDRAM from Samsung, AMD and SK Hynix. It is designed to be used in conjunction with high-performance graphics accelerators and network devices.[42] The first HBM memory chip was produced by SK Hynix in 2013.[43] Timeline See also: Random-access memory § Timeline, Flash memory § Timeline, and Transistor count § Memory SDRAM Synchronous dynamic random-access memory (SDRAM) Date of introduction Chip name Capacity (bits)[6] SDRAM type Manufacturer(s) Process MOSFET Area Ref 1992 KM48SL2000 16 Mbit SDR Samsung ? CMOS ? [4][3] 1996 MSM5718C50 18 Mbit RDRAM Oki ? CMOS ? 64 Mbit DDR Hyundai ? CMOS ? [10] 128 Mbit SDR Samsung ? CMOS ? [48][7] 1999 ? 128 Mbit DDR Samsung ? CMOS ? [7] 1024 Mbit DDR Samsung ? CMOS ? [46] 2000 GS eDRAM 32 Mbit eDRAM Sony, Toshiba 180 nm CMOS 279 mm2 [49] 2001 ? 288 Mbit RDRAM Hynix ? CMOS ? [50] ? DDR2 Samsung 100 nm CMOS ? [9][46] 2002 ? 256 Mbit SDR Hynix ? CMOS ? [50] 2003 EE+GS eDRAM 32 Mbit eDRAM Sony, Toshiba 90 nm CMOS 86 mm2 [49] ? 72 Mbit DDR3 Samsung 90 nm CMOS ? [51] 512 Mbit DDR2 Hynix ? CMOS ? [50] 2004 ? 2048 Mbit DDR2 Samsung 80 nm CMOS ? [53] 2005 EE+GS eDRAM 32 Mbit eDRAM Sony, Toshiba 65 nm CMOS ? [51] 2008 ? 16384 Mbit DDR3 Samsung 80 nm CMOS ? [55] ? 512 Mbit DDR3 Samsung 50 nm CMOS ? [55] ? 512 Mbit DDR3 Samsung 50 nm CMOS ? [55] ? 512 Mbit DDR3 Samsung 50 nm CMOS ? [57] 2008 ? 16384 Mb 2009 ?? DDR3 Hynix 44 nm CMOS ? [50] 2048 Mbit DDR3 Hynix 40 nm 2011 ? 16384 Mbit DDR3 Hynix 40 nm CMOS ? [43] 2013 ?? LPDDR4 Samsung 20 nm CMOS ? [43] 2013 ?? LPDDR5 Samsung 10 nm FinFET ? [59] 128 Gbit DDR4 Samsung 10 nm FinFET ? [60] SGRAM and HBM Synchronous graphics random-access memory (SGRAM) and High Bandwidth Memory (HBM) Date of introduction Chip name Capacity (bits)[6] SDRAM type Manufacturer(s) Process MOSFET Area Ref November 1994 HM5283206 8 Mbit SGRAM (SDR) Hitachi 350 nm CMOS 58 mm2 [38][61] December 1994 µPD481850 8 Mbit SGRAM (SDR) NEC ? CMOS 280 mm2 [39][41] 1997 µPD4811650 16 Mbit SGRAM (SDR) NEC 350 nm CMOS 280 mm2 [62][63] September 1998 ? 16 Mbit SGRAM (GDDR) Samsung ? CMOS ? [8] 1999 KM4132G112 32 Mbit SGRAM (SDR) NEC ? CMOS 280 mm2 [62][63] September 1998 ? 16 Mbit SGRAM (GDDR) Samsung ? CMOS ? [8] 1999 KM4132G112 32 Mbit SGRAM (SDR) NEC ? CMOS ? [64] 2002 ? 128 Mbit SGRAM (GDDR2) Samsung ? CMOS ? [65] 2003 ? 256 Mbit SGRAM (GDDR2) Samsung ? CMOS ? [65] 2003 ? 256 Mbit SGRAM (GDDR4) Hynix ? CMOS ? [50] SGRAM (GDDR3) March 2005 ? 256 Mbit SGRAM (GDDR4) Hynix ? CMOS ? [50] 2007 ? 1024 Mbit SGRAM (GDDR5) Hynix 60 nm 2009 ? 2048 Mbit SGRAM (GDDR5) Hynix 40 nm 2010 K4W1G1646G 1024 Mbit SGRAM (GDDR3) SK Hynix ? CMOS ? [43] 2013 ? ? HBM March 2016 MT58K256M32 A 8 Gbit SGRAM (GDDR5X) Micron 20 nm CMOS 140 mm2 [69] June 2016 ? 32 Gbit HBM2 Samsung 20 nm CMOS ? [70][71] 2017 ? 64 Gbit HBM2 Samsung 20 nm CMOS ? [70] January 2018 K4ZAF325BM 16 Gbit SGRAM (GDDR6) Samsung 10 nm FinFET 225 mm2 [72][73][74] See also GDDR (graphics DDR) and its subtypes GDDR2, GDDR3, GDDR4, and GDDR5 List of device bandwidths Serial presence detect - EEPROM with timing data on SDRAM modules SDRAM Tutorial - Flash website built by Tel-Aviv University students A concise but thorough review of SDRAM architecture/terminology and command timing dependencies in High-Performance DRAM System Design Constraints and Considerations, a master thesis from the University of Maryland. Notes References ^ P. Darche (2020). Microprocessor: Prolegomenes - Calculation and Storage Functions - Calculation Models and Computer. p. 59. ISBN 9780786305633. ^ B. Jacob; S. W. Ng; D. T. Wang (2008). Memory Systems: Cache, DRAM, Disk. Morgan Kaufmann. p. 324. ISBN 9780080553849. { {cite book} : CS1 maint: uses authors parameter (link) ^ a b c "Electronic Design". Electronic Design". Electronic Design. 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